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DERWENT-WEEK: 199042

TITLE: Plasma treatment of semiconductor wafer backside and appts. - by locating the wafer with its back side spaced from plasma-generating cathode

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INT-CL (IPC): C23C014/02, C23C016/02 , H01J037/32 , H01L021/00

ABSTRACTED-PUB-NO: EP 392134A

BASIC-ABSTRACT:

Back side of a semiconductor wafer is treated by locating the wafer with its back side spaced from a cathode; and forming a plasma in the space to treat the wafer back side.

Pref. the spacing is 0.8-2.5 cm., the pressure is 50-100 m. torr, and an RF power of 25-100W is applied for 10 sec. to 3 mins. to confine the plasma to the wafer back side.

USE - In removing impurities, including moisture, from the wafer back side and/or to inhibit undesired deposition of materials onto the back side.

ABSTRACTED-PUB-NO: US 4962049A

EQUIVALENT-ABSTRACTS:

A process for treating the back side of a semiconductor wafer, so that it does not interfere with future device processing operations, comprises supporting the wafer with this side near a cathode, and forming a plasma in the cathode/back side gap. Also calimed is a process as above comprising forming a protective oxide layer 10-30 A thick, which inhibits subsequent undesirable deposition, by working in a vacuum chamber with a gap. of 1/4-1 in. flowing oxidising gas at 50-200 sccm, and forming the plasma. Further claimed is a process as above in which the vacuum is 20-300 mtorr, the gas flow is 20-200 sccm, the r.f. energy of the plasma is 25-100W and it is maintained for 10-180's to form 10-30A of oxide layer. Additionally claimed is a process as the second above not specifying the gap size or the formation of an oxide layer. Also claimed is a process as the second above using an inert gas flow to remove undesirable material from the back side. Further claimed, is a process as the second above comprising forming a protective oxide layer which inhibits the subsequent deposition of undesirable matter. USE/ADVANTAGE - A method of treating the back side of a wafer so that materials which might interfere with subsequent front side IC processing are absent is provided. Materials already are removed from the deposition of e.g. W is prevented by an oxide coating which stops the formation of poorly adherent silicides which may flake off. The method is thus useful for IC processing in general.

CHOSEN-DRAWING: Dwg.2/3 Dwg.1/3

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DERWENT-CLASS: L03 U11 V05

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(54) Process and apparatus for treatment of backside of semiconductor wafer.

(57) A process and an apparatus are disclosed for the treatment of the backside or back surface of a semiconductor wafer such as a silicon wafer. By spacing the back side of a semiconductor wafer a predetermined distance from a cathode in a vacuum chamber and controlling the rf power and the pressure, a confined plasma may be used both to clean the back side of the wafer to remove impurities, including moisture and other occluded gases; as well as to deposit a layer of oxide on the back surface of the wafer to inhibit subsequent deposition of poorly adherent materials on the back side of the wafer which might otherwise flake off during processing of the front side of the wafer to form integrated circuits thereon.

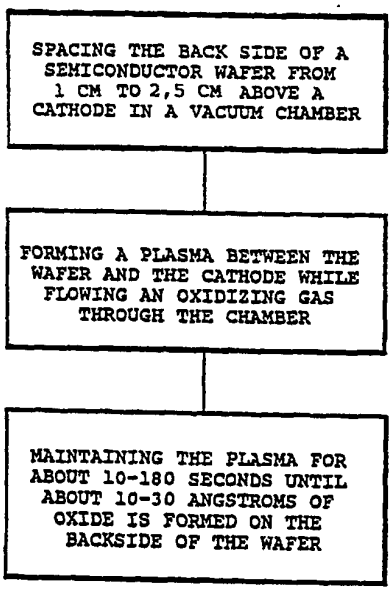


FIG. 1

EP 0 392 134 A2

PROCESS AND APPARATUS FOR TREATMENT OF BACKSIDE OF SEMICONDUCTOR WAFER

Background of the Inv ntion

1. Field of the Invention

This invention relates to a process and an apparatus for treating the backside of a semiconductor wafer according to the precharacterizing part of claim 1 and 7, respectively.

2. Description of the Related Art

In the formation of integrated circuit structure on a semiconductor wafer such as a silicon wafer, a number of different materials are deposited, patterned, and etched during the construction of the integrated circuits on the wafer.

During each of these steps, it is of utmost importance that no foreign materials, including dust or dirt particles, be in contact with the surface of the wafer, since precise alignment of each patterned layer is essential and the presence of any foreign materials could interfere with the deposition of a layer by causing imperfections in the layer, as well as interfere with the photolithography or etching steps.

In particular, it has been found that if a coating material such as tungsten is deposited on the integrated circuit structure, deposition of a layer of tungsten on the backside of the silicon wafer may occur as well. Unfortunately, this layer of tungsten which deposits on the backside of a silicon wafer adheres rather poorly, resulting in the flaking off of portions of the tungsten from the backside of the wafer. This, in turn, results in the deleterious formation of loose particles which interfere with the remainder of the processing as described above.

It has also been noted that the backside of a semiconductor wafer often comprises minor amounts of foreign materials, including moisture, which must be removed prior to placing the wafer in a high vacuum environment to avoid long baking or outgassing times.

Summary of the Invention

Therefore, it is the main object of the invention to provide a proc ss and an apparatus which would be capable of removing undesirable impurities from the backside of a semiconductor wafer and/or inhibit the deposit of undesirable materials onto the backside of the wafer as well.

Basically this invention provides a process and an apparatus for treating the backside of a semiconductor wafer in a manner which will result in the absence of materials on the backside of the wafer which would otherwise interfere with subsequent processing of the front side of the wafer to form integrated circuit structures thereon.

More specifically the invention provides a process and an appartus for treating the backside of a silicon wafer to form a coating, preferably an oxyde coating, thereon which will inhibit the deposition of materials, such as tungsten thereon which would react with the silicon to form a poorly adherent silicide coating thereon.

Alternatively this invention provides a process and an apparatus for treating the backside of a semiconductor wafer to remove materials present on the backside of the wafer which would otherwise interfere with subsequent processing of the front side of the wafer to form integrated circuit structures thereon.

The invention is characterized in claim 1 and 7, respectively.

Preferred embodiments of the invention are claimed in the rest of the subclaims.

Brief Description of the Drawings

Figure 1 is a flow sheet describing the process of the invention

Figure 2 is a vertical fragmentary cross-sectional view of apparatus used in the treatment of the backside of the wafer showing the use of support pins to space the underside of the wafer from the cathode.

Figure 3 is a top view of the semiconductor wafer shown in Figure 2, illustrating a typical positioning or array of the support pins beneath the wafer.

Detailed Description of the Invention

The invention provides a process for the treatment of the backside or back surface of a semiconductor wafer such as a silicon wafer. A plasma may be used both to clean the back side of the wafer to r move impurities, including moisture and other occluded gases, as well as to deposit a layer of oxide on the back surface of the wafer to inhibit subsequent deposition of poorly adherent materials on the back side of the wafer which might other-

wise flake off during processing of the front side of the wafer to form integrated circuits thereon.

The terms "backside" or "back surface", when referring to the semiconductor wafer used in the formation of integrated circuit structures, is intended to refer to the non-polished side of the wafer, while the top surface of the wafer refers to that surface of the semiconductor wafer which is normally polished to provide a very flat surface to facilitate subsequent formation of integrated circuit structures thereon.

Referring to Figures 2 and 3, a portion of a plasma etching chamber apparatus is shown comprising a conductive cathode 10 surrounded by insulation means 20. Positioned over cathode 10 is a semiconductor wafer 30 having a top surface 32 and a bottom surface 34. Pins 14 protrude upwardly from the surface of cathode 10 to support wafer 30 thereon a spaced distance from cathode 10 of from about 1 cm to about 2,5 cm to permit formation of a plasma therebetween as will be described below.

Pins 14 are provided with pointed ends 16 to engage the bottom surface 34 of wafer 30 while shielding a minimum area of surface 34. Pins 14 optionally may be retractable into recesses 12 in cathode 10 when not in use, as shows Figure 2. As shown in Figure 3, four such pins may be used to space wafer 30 from cathode 10. Other configurations and numbers of support pins can, of course, be used. Pins 14 may be made of any material which will not interefere with the processing of wafer 30. In one embodiment, pins 14 may be constructed of aluminum.

In accordance with the invention, the plasma etch chamber containing wafer 30 is maintained at a pressure of from about 50 to about 300 millitorr and a plasma is ignited between the backside surface 34 of wafer 30 and cathode 10 using conventional rf power generation equipment (not shown) operated at a power range of from about 25 to 100 watts.

In accordance with one aspect of the invention, during ignition of the plasma, a stream of an inert gas such as argon, neon, or helium is flowed through the etching chamber at a rate of about 20 to about 200 ccm/s. The plasma is maintained for a period of from about 10 to about 60 seconds which is sufficient to remove undesirable impurities, including moisture and other occluded gases from surface 34 of wafer 30. Wafer 30 may then be moved to a high vacuum chamber for further processing without the need for lengthy heating and outgassing to remove such gases and moisture from the back surface of the wafer.

In accordance with the preferred embodiment of the invention, however, an oxidizing gas, rather than an inert gas, is flowed through the etch chamber during the plasma flow to permit formation of an oxide layer on the back surface 34 of wafer 30 to a thickness of from about 10 to about 30 Angstroms, preferably about 20 to about 30 Angstroms, which is sufficient to inhibit the deposition of tungsten or other undesirable materials on back surface 34 of wafer 30 during subsequent processing of wafer 30. As in the cleaning embodiment, the length of time needed to form the oxide layer ranges from about 10 seconds to about 3 minutes, preferably from about 10 seconds to about 60 seconds.

It should be noted that when the oxidizing embodiment of the process of the invention is being practiced, there is no need to clean surface 34 prior to the oxidation since the heat generated by ignition of the plasma has been found to be sufficient to remove any materials on surface 34 which would otherwise interfere with the formation of the desired oxide coating thereon.

Example of oxidizing gases which may be used in include O_2, N_2O, O_3, and CO_2. However, of these gases O_2 is the preferred oxygen source, because it is easily available and most efficient for oxidation.

It should be noted that the maximum spacing range of wafer 30 from cathode 10 and the maximum rf power range specified are both important from the standpoint of controlling the extent of the oxidation of back surface 34 of wafer 30. While a larger spacing or a higher power range will still result in oxidation of surface 34, the resulting plasma will will be harder to control and contain, resulting in oxidation of not only back surface 34 but front surface 32 of wafer 30 as well.

While some oxidation of front surface 32 of wafer 30 is inevitable during the back surface oxidation process of the invention, any oxidation of front surface 32 must be removed to permit processing of the front surface to construct the desired integrated circuit structures therein. Therefore, it is preferable to form the desired oxidation layer on back surface 34 of wafer 30 under conditions which will minimize the amount of oxide formed on front surface 32.

While temperatures higher than room temperature, e.g., higher than about about 20 to about 25°C, may be used during the oxidation process, it is preferable to maintain a temperature not exceeding about 25°C in the plasma chamber for the same reasons as discussed above with regard to the maximum spacing and power level, i.e., to control the extent of the oxidation and to minimize oxidation of front surface 32 of wafer 30. The temperature in the plasma chamb r may be conveniently controlled by the temperature of the gas which is flowed into the chamber, or preferably by using a closed loop of chilled water flowing through

the chamber.

It should also be noted that it is pr f rable that the back side processing of the wafer in accordance with th invention be carried out prior to processing of the front side of the wafer to avoid interfering with any processing already carried out on the front side. However, when the protective oxide layer is formed on the back side surface of the wafer in accordance with the invention, subsequent processing of the front side of the wafer must be carried out in a selective manner which will not result in damage to the oxide layer on the back side of the wafer, such as subsequent wet etching of the front surface to remove oxide.

The following examples will serve to further illustrate the process of the invention.

Example I

A 12,5 cm diameter silicon wafer was spaced on pins 2,5 cm above a cathode in a plasma chamber evacuated to a pressure of 200 millitorr with the polished side of the wafer facing the cathode to facilitate measurement of the thickness of the oxide formed. While 100 ccm/s of O_2 were flowed through the chamber, a plasma was ignited between the cathode and the silicon wafer and then maintained at a power level of 75 watts for 60 seconds. The same procedure was then followed with a second wafer, however with the polished side facing away from the cathode to facilitate measurement of the thickness of the oxide formed on the opposite side of the wafer.

Subsequent measurement of the oxide thicknesses on the two wafers showed that an oxide layer of about 12-20 Angstroms thickness was formed on the polished side of the first wafer facing the cathode, while only about 6 Angstroms of oxide was formed on the polished side of the second wafer facing away from the cathode.

Example II

To illustrate the use of N_2O, instead of O_2 as the oxidizing gas, silicon wafers were processed using the procedure of Example I at a pressure of 20 millitorr, and a power level of 20 watts. N_2O was flowed through the chamber at a rate of 50 ccm/s and the plasma was maintained for 1 minute. Subsequent examination of the wafers showed that about 6-8 Angstroms of oxide were formed on the side of the wafer facing the cathode while 3 Angstroms of oxide were formed on the side of the wafer facing away from the cathode.

EXAMPLE III

To illustrate the difference in deposition of tungsten on a wafer having the backside oxide coating formed in accordance with the invention and a wafer not so treated, a silicon wafer having a 10-20 Angstrom oxide layer formed thereon in accordance with the procedure of Example I and a second silicon wafer not so treated were exposed to a deposition of tungsten by flowing 20 ccm/s of WF_6 gas for 1 minute through a vacuum chamber maintained at 10 Torr and 300° C. Subsequent examination of the two wafers under a microscope showed no reflectivity change on the surface of the wafer coated with oxide in accordance with the invention, while the wafer not so treated showed the surface converted to tungsten almost completely.

Thus, the invention provides a process for treating the back side of a semiconductor wafer which is capable of removing undesirable impurities from the backside of a semiconductor wafer and inhibiting the deposit of undesirable materials onto the backside of the wafer as well.

Claims

1. A process for treating the back side of a semiconductor wafer which comprises:

a) supporting a semiconductor wafer a spaced distance from a cathode with the back side of said wafer facing said cathode; and

b) forming a plasma in the gap formed between said cathode and said back side of said wafer to treat said back side of the semiconductor wafer.

2. The process of claim 1, wherein said step of supporting a semiconductor wafer a spaced distance from a cathode further comprises spacing said back side of said wafer a distance of from about 0.8 cm to about 2.5 cm from said cathode.

3. The process of claim 1 or 2, wherein said process is carried out in a vacuum chamber maintained at a vacuum of from about 50 to about 100 millitorr.

4. The process of claim 1, 2 or 3, wherein said step of forming a plasma further comprises maintaining the rf power at from about 25 to about 100 watts for a period of from about 10 second to about 3 minutes to substantially confine said plasma to the back side of said wafer.

5. The process of any of claims 1 to 4, wherein said step of forming said plasma further includes flowing an inert gas selected from the class consisting of argon, neon and helium through said chamber at a rate of from about 50 to about 200

ccm/s.

6. The process of any of claims 1 to 4, wherein said step of forming said plasma further includes flowing an oxidizing gas selected from the class consisting of O_2, N_2O, O_3 and CO_2 through said chamber at a rate of from about 20 to about 200 ccm/s to form from about 10 to about 30 Angstroms of an oxide layer on said back side of said wafer.

7. An apparatus for treating the back side of a semiconductor wafer comprising:
- a vacuum chamber;
- a cathode (10) arranged in said vacuum chamber;
- support means (14) for punctual the engaging said back side of said semiconductor wafer protruding upwardly from said cathode (10) within said chamber; and
- a gas supply means for supplying an inert gas or an oxidizing gas through said chamber in order to form a plasma in the gap formed between said cathode and said back side of said wafer.

8. The apparatus of claim 7, wherein said support means comprises pins (14) spacedly arranged to each other.

9. The apparatus of claim 7 or 8, wherein said support means or said pins (14) respectively, are arranged retractable into recesses (12) formed in said cathode (10).

10. The apparatus of any of the claims 7 to 9, wherein said vacuum chamber is connected to a means for maintaining a vacuum from about 50 to about 300 millitorr in said vacuum chamber.

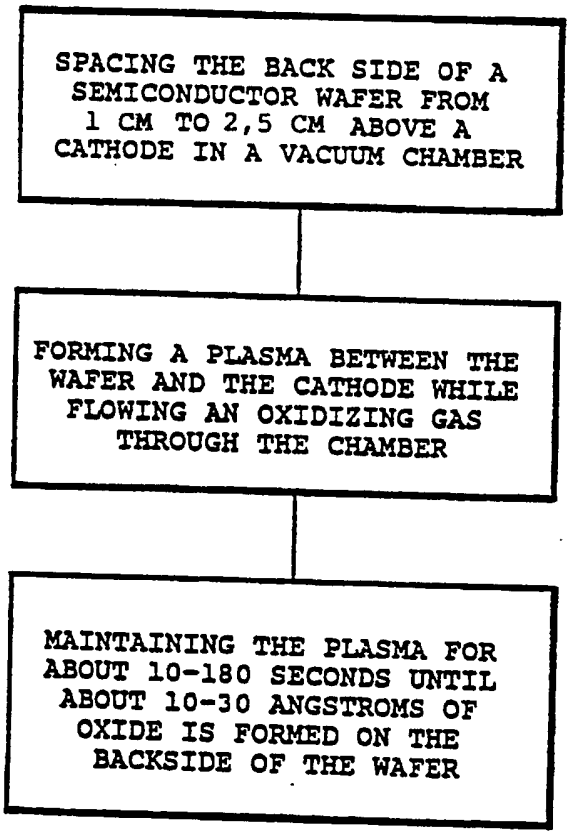

SPACING THE BACK SIDE OF A SEMICONDUCTOR WAFER FROM 1 CM TO 2,5 CM ABOVE A CATHODE IN A VACUUM CHAMBER
FORMING A PLASMA BETWEEN THE WAFER AND THE CATHODE WHILE FLOWING AN OXIDIZING GAS THROUGH THE CHAMBER
MAINTAINING THE PLASMA FOR ABOUT 10-180 SECONDS UNTIL ABOUT 10-30 ANGSTROMS OF OXIDE IS FORMED ON THE BACKSIDE OF THE WAFER

FIG. 1

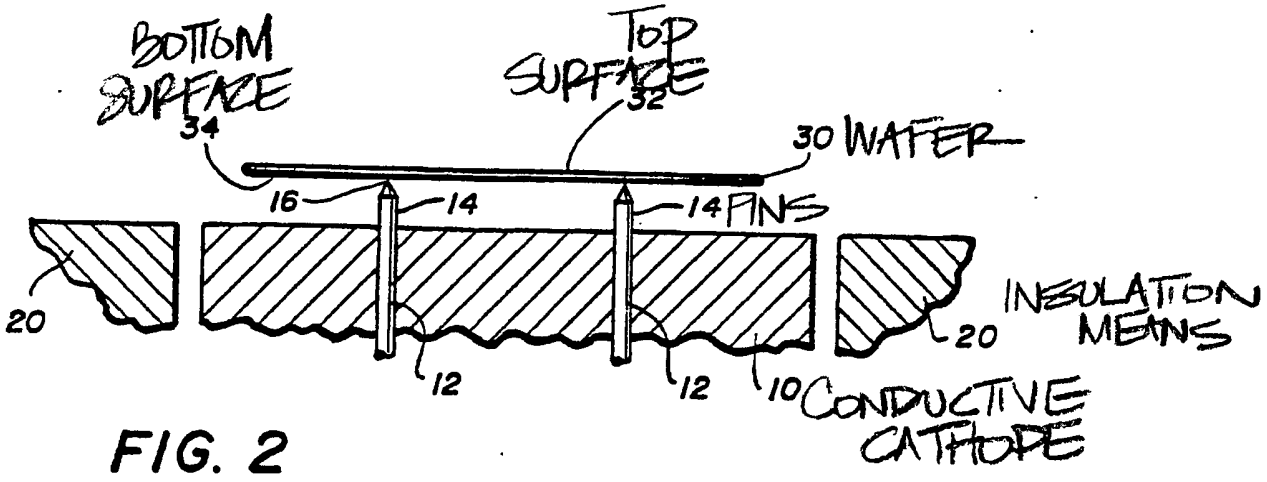
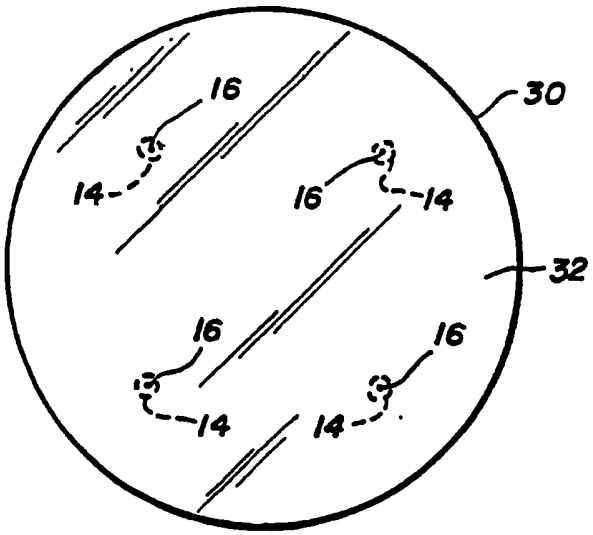

BOTTOM SURFACE
34
TOP SURFACE
32
30 WAFER
16
14
14 FINS
20
12
12
10
20
INSULATION MEANS
CONDUCTIVE CATHODE

FIG. 2

FIG. 3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